

1 (10) ABSTRACT

2 Electrostatic discharge protection for integrated circuits, particularly for enhancing
3 electrostatic discharge protection performance for Input-output cells and power supply
4 clamps used in CMOS and BiCMOS IC technologies is described. A P-type, implantation
5 region, or layer, referred to as "P-deep," in both N-MOSFET and P-MOSFET devices is
6 provided to enhance electrostatic discharge protection performance. Parasitic transistor
7 gain is enhanced by providing the P-deep region subposing the drain contact.
8 Exemplary embodiments for N-type and P-type MOSFETs, MOSFETs with surface
9 diodes, MOSFETS with SCRs, and push-pull Input-output CMOS circuits are described.